CURRICULUM VITAE

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April 2017

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Savvas Chamberlain a Distinguished Professor Emeritus of the University of Waterloo is presently the CEO and Chairman of EXEL Research Inc. a company which provides services to identify and commercialize innovations arising from university research. This company also invests in promising young high tech companies in Canada.

Savvas was born in Dhikomo, Cyprus, of Greek Cypriot heritage. He was educated in England, received his first degree in London, and his M.Sc. and Ph.D. degrees from Southampton University. After his Ph.D. in 1968 he worked briefly with Plessey Research Laboratories in Caswell, and then immigrated in 1969 to Canada. In 1974 he became a proud Canadian Citizen. In July 2009 Savvas was inducted into the Order of Canada. He is a resident of Ontario. In 1980 he founded DALSA, a successful Semiconductor and Electronics company in Canada.

Scientific and engineering contributions
The research work and achievements of Dr. Savvas Chamberlain extend from the mid 1960's to the mid 1990's. At the University of Waterloo while a Professor of Electrical and Computer Engineering, he pioneered new semiconductor device theories and developed innovative imaging semiconductor devices, together with their associated fabrication processes. The new devices offered superior electrical performance relative to existing technologies. He succeeded in integrating his original fundamental scientific contributions by introducing a holistic "Frame Transfer and Time-Delay-and-Integration Image Sensor CCD Technology". This technology can produce very high speed CCD image sensors and digital cameras with superior performance, in the areas of higher frame rate, higher photosensitivity, and higher dynamic range, all in relation to the then and present global state of the art.

These high performance semiconductor image sensors have found application in digital cameras for industrial applications such as high definition cameras, in postal sorting machines, in wafer inspection technologies, intelligent transport systems, and a host of other applications, including the CCD sensors used to capture and transmit to earth, for the first time, pictures from Mars by the first NASA's Mars Exploration Rover.

He published his research work in more than 118 refereed publications, and authored or coauthored more than 20 patents. His contributions have been globally recognized by the engineering and scientific community.

In the 1980's, he successfully transferred the technology which he invented and developed through his research work to DALSA Corporation. Using this technology new CCD and CMOS Image sensors with much superior performance were produced. DALSA is a globally recognized Canadian technology compann, (Now-2017 TeledyneDALSA).

Dr. Chamberlain has been awarded many honors; On July1, 2009 he was appointed to the Order of Canada for his contributions to Canada's reputation as a global leader in high performance imaging and semiconductors. The international Automated Imaging Association awarded him the ***Life Time Achievement Award*** in 2004 for his international

contributions and leadership in semiconductor image sensors and digital imaging. In 1991 he was elected a Fellow of IEEE for ***his contributions to CCD Imagers and MOS*FET's. I**n June 2007 Dr. Chamberlain was awarded an Honorary Doctor of Engineering Degree by the University of Waterloo for his ***industrial contributions***, and in April 2007 he received the Ontario Premier's Catalyst award for ***life time achievement in innovation.*** In May 2008 Dr. Chamberlain was elected a Fellow of The Canadian Academy of Engineering. In March 2009 he was inducted as Fellow of the Engineering Institute of Canada.

Other Contributions to Society: Training of Highly Qualified Personnel
While at the University of Waterloo, in the Electrical and Computer Engineering Department, in the early 1970's, and in collaboration with Professor David Roulston, Chamberlain established and set up the Silicon Devices and Integrated Circuits Microelectronics Fabrication Laboratory. This laboratory played a central role in the emergence of Waterloo as a major player in semiconductor materials and devices, serving as a cornerstone for the development of nanotechnology research and education at the University in 2000-2010.

As a Professor for more than twenty years Dr. Chamberlain used this laboratory to invent new semiconductor devices and to supervise, train and graduate 16 Ph.D.'s and 29 M.A.Sc students. Many of these graduates now have leading positions in international companies and Universities. This is a substantive contribution to the training of highly qualified engineers and scientists.

Creating Wealth and Jobs in Canada through Entrepreneurship and Innovation
Dr. Chamberlain founded DALSA Corporation in 1980. A semiconductor and electronics spin-off company from the University of Waterloo, DALSA had its head office and primary location in waterloo, Ontario. Other locations include: Montreal, Bromont Quebec, Netherlands, Munich Germany and Japan. The company grew rapidly and created high quality technology jobs in Canada and worldwide. More than 300 of these jobs were in Ontario and 500 in Quebec. Under Savvas' leadership the annual revenues of DALSA grew to $212 million. More than 95% of the revenues were derived from exports to countries such as the US, Asia Pacific countries and Europe. DALSA thus served as a role model for a university spin-off company and a globally competitive Canadian technology Enterprise. In February 12, 2011, three Hedge Funds forced Dr. Chamberlain to sell DALSA to Teledyne Technologies and it is now TeledyneDALSA.

Support for the Arts and Charitable Organizations

Savvas Chamberlain has been an exceptional supporter of charitable organizations and the arts. He has made significant donations to the Kitchener-Waterloo Symphony, the Opera and several other arts and culture projects. He set up a number of endowments for annual charitable contributions: the Savvas Chamberlain Scholarship endowment fund, and the Savvas Chamberlain Graduate Scholarship endowment fund, both, with the University of Waterloo for annual undergraduate and graduate scholarships in Electrical and Computer Engineering; the Lenia Chamberlain Memorial Graduate Scholarship with CFUW and Wilfrid Laurier University for an annual graduate scholarship in Culture and Religion; the Savvas and Lenia Chamberlain Endowment fund with the Kitchener-Waterloo Community Foundation for annual charitable donations in the Kitchener-Waterloo community. In February 2011 Savvas founded and funded **The Savvas Chamberlain**

Family Foundation, www.scffoundation.com This is a charitable organization which provides funding for projects for the underprivileged, education, health, arts and culture and the preservation of the environment.

Through professional interactions with the University of Waterloo, community leaders, and other Canadian Institutions, he contributes his time and experience to encourage and facilitate the formation of new technology companies and the growth of technology industry in Ontario, and Canada.

Savvas enjoys nature, walks and hikes, classical music, classical jazz, live theatre, opera, Greek literature, current events, gardening, traveling. He enjoys spending time with his wife Christine, his three children and his five grandchildren. His iPod has more than 3000 pieces of music, which includes, not only classical, but many Greek songs and music from throughout the world.

A. CURRICULUM VITAE

Savvas Chamberlain

ACADEMIC QUALIFICATIONS:

Doctorate:	Ph.D. 1968	Southampton University, U.K.
Masters:	M.Sc. 1965	Southampton University, U.K.
Other:	D.U.S. 1965	Southampton University, U.K.
Diploma in Electronics	July 1964	Northern Polytechnic, (Metropolitan University, London, UK.
Owner/President Management	1994	Harvard Business School.

EXEL Research Inc.

February 2011 to present, CEO and Chairman,

DALSA Corporation, Semiconductor and Electronics, Waterloo, Ontario, Canada

September 2007- February 2011, CTO and Chairman of the board and Founder.
1980 – August 2007, CEO and Chairman of the Board and Founder.

UNIVERSITY OF WATERLOO, Waterloo, Ontario, Canada

June 1999, Distinguished Professor Emeritus, Electrical and Computer Engineering.
1996 – 1999, Adjunct Professor, Electrical and Computer Engineering.
July 1977 – 1996, Full Professor, Electrical and Computer Engineering.
May 1988 – Sept. 1988, Acting Chairman, Electrical and Computer Engineering
Sept. 1982 – Aug. 1986, Associate Chairman – Graduate Studies, Electrical Engineering.
July 1972 – June 1977, Associate Professor, Electrical Engineering.
May 1969 – June 1972, Assistant Professor, Electrical Engineering.

IBM THOMAS J. WATSON RESEARCH CENTER, Yorktown Heights, N.Y.

Aug. 1981 – Sept. 1982, Visiting Scientist (full-time): Research on VLSI MOSFETs and CCD image sensors.

Oct. 1975 – Dec. 1985, IBM Independent Consultant: Scanners, photodetectors CCDs and integrated circuits.

Sept. 1974 – Sept. 1975, Visiting Scientist (full-time): Research on MOSFETs, photodetectors, CCD scanners, integrated circuits and systems.

BELL NORTHERN RESEARCH, Ottawa, Ontario, Canada

Sept. 1971 – Apr. 1972, Visiting Scientist (full-time): Design of Integrated Circuits, Research and Development of CCD Technology.

May 1972 – Aug. 1974, Independent Consultant: Semiconductor devices, design of integrated MOSFET circuits and CCDs.

PLESSEY CO. LTD., ALLEN CLARK RESEARCH CENTER, Caswell, U.K.

Jan. 1968 – Apr. 1969, Research Scientist: Development of Bi-polar and MOSFET semiconductor devices and design of integrated circuits.

HONOURS AND AWARDS:

Recognition awards for original scientific and engineering contributions:

- *Life time achievement award Communitech 2012*
- *Inducted in the Hall of Fame in Waterloo Region Entepreneur Hall of Fame, November 2012.*
- *Fellow of the Royal Society of Canada 2012.*
- *Appointed Member of the Order of Canada on July1, 2009.*
- *Inducted as a Fellow of the Canadian Engineering Institute in March 2009.*
- Inducted as a Fellow of the Canadian Academy of Engineering, July 2008
- Distinguished Professor Emeritus, Electrical and Computer Engineering, University of Waterloo, 1999
- ITAC/NSERC Award for Outstanding Research Contribution in Canada, April 1993.
- Elected Fellow of the Institute of Electrical and Electronics Engineers (IEEE) for his contributions to CCDs and MOSFETs, January 1, 1991.
- Honorary Doctor of Engineering Degree, University of Waterloo, June 2007.

Board Memberships

- *Chairman of the Board of Directors of EXEL Research Inc. 1980 to present*
- Chairman of the Scientific Advisory board of the Waterloo Institute of Nanotechnology of the University of Waterloo**.** 2009-present.
- *Chairman of the Board of Directors of Huron Technologies International Corp 2011-present.*
- Chairman of the Board of Directors of The Savvas Chamberlain Family Foundation December 2010-present
- *Chairman of the Board of Directors of Oak Tech Holdings, 2013-present*
- *Member of the Board of Directors of Pleora Technologies 2009-present*
- *Member of the Board of Directors TrustPoint Technologies 2014-March 2017*
- *Chairman of the Board of Directors of DALSA Corp, 1980 –Feb 2011. .*
- Member of the Board of Directors, CMC (Centre of Excellence), 2004 – June 2007.
- Member of the Board of Directors of SMC, (Strategic Microelectronics Corporation), Ottawa, ON, a non-profit body providing policy advice to the federal government), 1992 – 1999.

Other Board of Director Memberships and Advisory Boards

- Member of the advisory board of the Dean's Development Council, Dean of Engineering University of Waterloo. 2009-present.
- *Member of the advisory board of IMS, NRC, Ottawa. Jan 2009-2011.*
- Member of the advisory board of the Ontario Center of Excellence for commercialization of innovations. 2009 - 2012.
- Member of the Chairman's Council of the Kitchener-Waterloo Symphony.
- Member of the Board of Directors, Opera Ontario, 1999 – 2004.
- Member of the Board of Directors, Kitchener-Waterloo Symphony, 1998 – 2001.
- Member of the Board of Directors and Operations Committee of ICR until June 1995.

Recognition awards for original scientific contributions applied to industry:

- *ITAC Outstanding Service award in the area of Semiconductors and Photonics, October 2008.*
- Premier's Catalyst Award for Lifetime Achievement in Innovation from Ontario Premier and Minister of Research and Innovation Dalton McGuinty honoring Ontario's top research and innovation talents, April 2007.
- Automated Imaging Association, Life Achievement Award, in recognition of his worldwide influence on the image sensor and digital camera industry, 2004.
- Greater Kitchener-Waterloo Chamber of Commerce, Business Leader of the Year, 2004.
- Ernst &Young Ontario Entrepreneur-of-the-Year Award for Technology and Communications segment, 2003.

PROFESSIONAL ACTIVITIES:

- Member of the Canadian Academies Expert Panel on Business Innovation 2008
- *Expert panel on Innovation……. Canadian Council of Academies, xxx- July 2009. .*
- *Dean's advisory council, Faculty of Engineering, University of Waterloo.*
- Member of the Board of Directors of the Automated Imaging Association, an international professional organization, 1994 – 1996.
- Member of the organizing committee of the IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Japan, 1997-1999.
- Chairman of the NSERC Operating Grant Selection Committee, Electrical Engineering, 1988-1989.
- Member of the NSERC Operating Grant Selection Committee, Electrical Engineering, 1986-1987.
- Chairman of the committee for Detectors, Sensors and Displays, IEEE International Electron Devices Meeting Conference, 1997.
- Member of the IEEE IEDM Program Committee of Detectors, Sensors and Displays, 1994-1996.
- Conference Chairman of the IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Waterloo, ON, 1993-1995.

A. LIST OF PATENTS

1. ***S.G. Chamberlain and W.D. Washkurak, "Switched CCD Electrode Photodetector," United States Patent Office, USA Patent No. 5602407, Issued February 11, 1997.***

2. ***S.G. Chamberlain and W.D. Washkurak, "Dual Mode On-Chip High Frequency Output Structure with Pixel Video Differencing for CCD Image Sensors," United States Patent Office, USA Patent No. 5452003, Issued September 19, 1995.***

3. ***C.R. Selvakumar and S.G. Chamberlain, "Method for Making Silicon-Germanium Devices Using Germanium Implantation," United States Patent Office, USA Patent No. 5426069, Issued June 12, 1995.***

4. ***S.G. Chamberlain and W.D. Washkurak, "High Photosensitivity and High Dynamic Range CCD Image Sensor," United States Patent Office, USA Patent No. 720408, Issued August 10, 1993.***

5. ***S.G. Chamberlain, B.C. Doody, M. Meithig and W.D. Washkurak, "Electronically Expandable Modular CCD Camera," United States Patent Office, USA Patent No. 740226, Issued June 5, 1993.***

6. ***S.G. Chamberlain and W.D. Washkurak, "High Frame Rate CCD Imager with a New Fast Overall Reset," United States Patent Office, USA Patent No. 689782, Filed January 20, 1992.***

7. ***W.D. Washkurak and S.G. Chamberlain, "Area Image Sensors with On-Chip Electronics," United States Patent Office, USA Patent No. 699789, Filed February 27, 1992.***

8. ***W.D. Washkurak and S.G. Chamberlain, "Surface Clocked Antiblooming Technique for Area Array CCD Image Sensors," United States Patent Office, Filed June 1, 1992.***

9. ***W.D. Washkurak and S.G. Chamberlain, "A 6032 x 32 Time-Delay and Integration (TDI) Abuttable Image Sensor," United States Patent Office, Filed May 5, 1992.***

10. ***S.G. Chamberlain and E.S. Schlig, "Absolute charge difference detection method and structure for a charge coupled device," United States Patent Office, USA Patent No. 4639678, Issued January 1987.***

11. ***S.G. Chamberlain, G. Rhorer and K.S. Pennington, "On-Chip CCD Realization of the Laplacian Operator for Image Signal Processing," United States Patent Office, USA Patent No. 4568977, Issued February 4, 1986.***

12. ***S.G. Chamberlain and E.S. Schlig, "Charge-Coupled Device Output Circuit Structure," United States patent Office, USA Patent No. 4513431, Issued April 1985.***

13. ***S.G. Chamberlain, "Integrable large dynamic range photodetector element for linear and area integrated circuit imaging arrays," United States Patent Office, USA Patent No. 4473836, Issued September 25, 1984.***

14. ***S.G. Chamberlain, "Integrable large dynamic range photodetector element for linear and area integrated circuit imaging arrays," Canadian Patent Office, Patent No. 400608, Issued August 28, 1984.***

15. ***S.G. Chamberlain, "Photoelement with improved blue color response," Canadian Patent Office, Patent No. 1090457, Issued November 25, 1980.***

16. ***S.G. Chamberlain and L.G. Heller, "Photoelement with improved linearity," France Patent Office, Patent No. 7736922, Issued November 8, 1980.***

17. ***S.G. Chamberlain and L.G. Heller, "Photoelement with improved linearity," United Kingdom Patent Office, Patent No. 1592373, Issued April 30, 1979.***

18. ***S.G. Chamberlain, "Photoelement with improved blue color response," France Patent Office, Patent No. 7720045, Issued August 14, 1979.***

19. ***S.G. Chamberlain and D.H. Harper, "Photogeneration Channel in Front Illuminated Solid-State Silicon Imaging Devices," Canadian Patent Office, Patent No. 1060566, Issued August 14, 1979.***

20. S.G. Chamberlain, "Photoelement with improved blue color response," United States Patent Office, Patent No. 4107722, Issued August 15, 1978.

21. S.G. Chamberlain and D.H. Harper, "Photogeneration Channel in Front Illuminated Solid-State Silicon Imaging Devices," United States Patent Office, Patent No. 4025943, Issued May 2, 1977.

22. S.G. Chamberlain and L.G. Heller, "Highly Sensitive Charge-Coupled Photodetector," United States Patent Office, Patent No. 4019199, Issued April 19, 1977.

Authorship Sequence

It has been the Policy of Dr. Savvas Chamberlain to put the names of his students first on the papers if they participated in his research.

B. FULL PAPERS PUBLISHED IN REFEREED JOURNALS

1. S.M. GadelRab, S.G. Chamberlain, "Thick-Layered Etched-Contact Amorphous Silicon Transistors," *IEEE Transactions on Electron Devices*, Vol. 45, No. 2, pp. 465-471, February 1998.

2. S.M. GadelRab, A.M. Miri, S.G. Chamberlain, "A Comparison of the Performance and Reliability of Wet-Etched and Dry-Etched a-Si:H TFT's," *IEEE Transactions on Electron Devices*, Vol. 45, No. 2, pp. 560-563, February 1998.

3. S.M. GadelRab, S.G. Chamberlain, "The Source-Gated Amorphous Silicon Photo-Transistor," *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp. 1789-1794, October 1997.

4. A.M. Miri, S.G. Chamberlain, A. Nathan, "Effects of Deposition Power and Temperature on the Properties of Heavily Doped Microcrystalline Silicon Films," *Mat. Res. Soc. Symp. Proc*., Vol. 420, pp. 307-312, 1996.

5. A.M. Miri, P.S. Gudem, S.G. Chamberlain, A. Nathan, "A Novel Device Structure for High Voltage, High Performance of Amorphous Silicon Thin-Film Transistors," *Mat. Res. Soc. Symp. Proc*., Vol. 420, pp. 93-98, 1996.

6. S.M. GadelRab, S.G. Chamberlain, "The effects of metal-n^+ interface and space charge limited conduction on the performance of amorphous silicon thin-film transistors," *IEEE Transactions on Electron Devices*, Vol. 41, pp. 462-464, 1994.

7. D.A.B. Dobson, S.G. Chamberlain, "Transient Analysis of Signal Charge Transfer in Long Diffused Regions of Spectroscopic Image Sensors*," Canadian Journal of Physics*, Vol. 70, pp. 1086-1091, 1993.

8. J.W. Roberts, S.G. Chamberlain, "An Experimental Procedure for Measuring Silicon Lattice Heating to Hot Carriers in MOSFETs*," Solid-State Electronics*, Vol. 36, No. 3, pp. 351-360, 1993.

9. S. Agwani, S.G. Chamberlain, J.R.F. McMacken, B. Leung, "Compact Model for Small Geometry MOSFETs," *Canadian Journal of Electrical and Computer Engineering*, August 1992.

10. J.R.F. McMacken, S.G. Chamberlain, “A Numerical Model for Two-Dimensional Transient Simulation of Amorphous Silicon Thin-Film Transistors,” *IEEE Transactions On Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, pp. 801-815, April 1992.

11. C.R. Smith, S.G. Chamberlain, “Theory and design Methodology for an Optimum Single-Phase CCD,” *IEEE Transactions on Electron Devices*, Vol. 39, pp. 864-873, April 1992.

12. S.H. Hood, S.G. Chamberlain, “Color Filter Arrays for Silicon Solid-State Image Array Sensors,” *Canadian Journal on Physics*, Vol. 69, No. 3 & 4, pp. 543-548, March/April 1991.

13. J.W. Roberts, S.G. Chamberlain, J.R.F. McMacken, “Energy-Momentum Transport Based Simulator Adapted to CHORD,” *Canadian Journal of Physics*, Vol. 69, No. 3 & 4, pp. 217-223, March/April 1991.

14. J.R.F. McMacken, S.G. Chamberlain, “Analytic and Iterative Transit Models for VLSI MOSFETs in strong inversion,” *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 5, pp. 1257-1267, October 1990.

15. J.W. Roberts, S.G. Chamberlain, “Energy-Momentum Transport Model for Small Geometry Silicon Device Simulation,” *COMPEL, International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, Vol. 9, No. 1, pp. 1-22, March 1990.

16. J.W. Roberts, S.G. Chamberlain, “A CMOS model for computer aided circuit analysis and design,” *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 1, pp. 128-138, 1989.

17. P.A. Layman, S.G. Chamberlain, “A Compact Thermal Noise Model for the Investigation of Soft Error Rate in MOS VLSI Digital Circuits,” *IEEE Journal of Solid-State Circuit*s, Vol. 24, No. 1, pp. 79-89, 1989.

18. M.J. Van der Tol, S.G. Chamberlain, “Potential and Electron Distribution Model for the Buried-Channel MOSFET,” *IEEE Transactions on Electron Devices*, Vol. 36, No. 4, pp. 670-689, 1989.

19. J.R.F. McMacken, S.G. Chamberlain, “CHORD: A Modular Semiconductor Device Simulation Development Tool Incorporating External Network Models,” *IEEE Transactions on Computer-Aided Design*, Vol. 8, No. 8, pp. 826-836, 1989.

20. R. Inkol, W.D. Washkurak, S.G. Chamberlain, “A photodetector array for acousto-optic signal processors,” *Canadian Journal of Physics*, Vol. 67, pp. 1-8, 1989.

21. B.C. Doody, S.G. Chamberlain, “ An improved wide dynamic range silicon photodetector for integration in image sensor arrays*,” Canadian Journal of Physics*, Vol. 65, No. 8, pp. 919-923, 1987.

22. S.G. Chamberlain, S. Ramanan, “Drain Induced Barrier Lowering Analysis in VLSI MOSFET Devices Using Two-Dimensional Numerical Simulations,” *IEEE Transactions on Electron Devices*, Vol. ED-33, No. 11, pp. 1745-1753, 1986.

23. S.G. Chamberlain, J.P.Y. Lee, “A novel wide dynamic range silicon photodetector and linear imaging array,” *IEEE Transactions on Electron Devices*, Vol. ED-31, pp. 175-182, 1984.

24. S.G. Chamberlain, A. Husain, F.H. Gaensslen, “Nonuniform Displacement of MOSFET Channel Pinchoff,” *IEEE Transactions on Electron Devices*, Vol. ED-31, pp. 252-256, 1984.

25. R. Kumar, S.G. Chamberlain, D.J. Roulston, “Two-Dimensional Computer Simulation of the breakdown characteristics of a Multi-Element Avalanche Photodiode Array,” *IEEE Transactions on Electron Devices*, Vol. ED-31, pp. 828- 833, 1984.

26. K.V. Anand, S.G. Chamberlain, “A Novel p-n Junction Polycrystalline Silicon Gate MOSFET,” *International Journal of Electronics*, Vol. 54, No. 2, pp. 287-298, 1983.

27. K.V. Anand, S.G. Chamberlain, “Novel p-n junction polysilicon dual-gate MOSFET for analogue applications,” *IEE Proceedings*, Vol. 129, Pt. I, No. 2, pp. 58-60, 1982.

28. A. Husain, S.G. Chamberlain, “Three Dimensional Simulation of VLSI MOSFETs: The Three-Dimensional Simulation Program WATMOS,” *IEEE Transactions on Electron Devices*, Vol. ED-29, NO. 4, pp. 631-638, April 1982.

29. D.J. Roulston, N.D. Arora, S.G. Chamberlain, “Modeling and Measurement of Minority-carrier Lifetime versus Doping in Diffused Layers of n+-p Silicon Diodes,” *IEEE Transaction on Electron Devices*, Vol. ED-29, No. 2, pp. 284-291, 1982.

30. H.S.A. Zohdy, S.G. Chamberlain, “The development and application of the correlation method for noise spectral intensity measurements in Sampled-Data Circuits,” *IEEE Transactions on Instrumentation and Measurement*, Vol. IM-8, pp. 1-12, 1982.

31. R. Kumar, S.G. Chamberlain, “Bulk charge effects in VLSI MOSFETs,” *Solid-State Electronics*, Vol. 24, No. 11, pp. 1071-1074, 1981.

32. M.H. El-Diwany, D.J. Roulston, S.G. Chamberlain, “Design of Low-Noise Bipolar Trans-impedance Preamplifiers for Optical Receivers,” *IEE Proceedings*, Vol. 128, Pt. G., No. 6, pp. 299-306, 1981.

33. R. Kumar, D.J. Roulston, S.G. Chamberlain, “Two-Dimensional Simulation of a High-Voltage p-i-n Diode with overhanging Metalization,” *IEEE Transactions on Electron Devices*, Vol. ED-28, No. 5, pp. 534-540, 1981.

34. R. Kumar, S.G. Chamberlain, D.J. Roulston, “An algorithm for two dimensional simulation of reverse-biased beveled p-n junction,” *Solid-State Electronics*, Vol. 24, pp. 309-311, 1981.

35. R. Kumar, D.J. Roulston, S.G. Chamberlain, “Accurate Two-Dimensional Simulation of Double-Beveled p-n Junctions,” *Solid-State Electronics*, Vol. 24, pp. 377-370, 1981.

36. H.S.A. Zohdy, S.G. Chamberlain, L.A.K. Watt, “Limitations of Multilevel Storage in Charge-Coupled Devices,” *IEEE Transaction on Electron Devices*, Vol. ED-27, pp. 1559-1575, September 1980.

37. S.G. Chamberlain, “Advances in CCD Scanners with On-Chip Signal Processing for Electronic Imaging,” *The Radio and Electronic Engineer*, Vol. 50, pp. 249-257, May 1980.

38. D.B. Scott, S.G. Chamberlain, “Modeling and Experimental Simulation of the Low-Frequency Transfer Inefficiency in Bucket-Brigade Devices,” *IEEE Transactions on Electron Devices*, Vol. ED-27, pp. 405-414, February 1980.

39. R.J. Inkol, S.G. Chamberlain, “Design and Realization of a Two-Level 64k byte CCD Memory System for Microcomputer Applications,” *IEEE Journal of Solid-State Circuits*, Vol. SC-15, pp. 131-135, February 1980.

40. S.G. Chamberlain, “New Profiled Silicon Photodetector for Improved Short-Wavelength Quantum Efficiency,” *Journal of Applied Physics*, Vol. 50, pp. 7228-7232, November 1979.

41. D.B. Scott, S.G. Chamberlain, “A Calibrated Model for the Subthreshold Operation of Short Channel MOSFET Including Surface States,” *IEEE Journal of Solid-State Circuits*, Vol. SC-14, pp. 633-644, June 1979.

42. S.G. Chamberlain, D.J. Roulston, S.P. Desai, “Spectral Response Limitation Mechanisms of a Shallow Junction n+-p Photodiode,” *IEEE Transactions on Electron Devices*, Vol. ED-25, pp. 241-246, February 1978.

43. S.G. Chamberlain, D.H. Harper, “MTF Simulation Including Transmittance Effects and Experimental Results of Charge Coupled Imagers,” *IEEE Journal of Solid-State Circuits*, Vol. SC-13, pp. 71-80, February 1978.

44. J.M. White, S.G. Chamberlain, “A Multiple-Gate CCD Photodiode Sensor Element for Imaging Arrays,” *IEEE Transactions on Electron Devices*, Vol. ED-25, pp. 125-131, 1978.

45. M.H. Elsaid, S.G. Chamberlain, “Short-Channel Effects on the Input Stage of Surface-Channel CCDs,” *IEEE Transactions on Electron Devices*, Vol. ED-24, pp. 1164-1171, September 1977.

46. D.B. Scott, S.G. Chamberlain, “Experimental Confirmation of an Analytical Model for Charge Transfer in Charge-Coupled Devices,” *IEEE Journal of Solid State Circuits*, Vol. SC-12, pp. 1-15, 1977.

47. R.C. Kumar, D.J. Roulston, S.G. Chamberlain, “A Study of the Effect of Peripheral Injection in Bipolar Transistors Using Simplified Computer Analysis,” *IEEE Transactions on Electron Devices*, Vol. ED-24, pp. 1-12, March 1977.

48. M.H. Elsaid, S.G. Chamberlain, L.A.K. Watt, “Computer Model and Charge Transport Studies in Short Gate Charge-Coupled Devices,” *Solid-State Electronics*, Vol. 20, pp. 61-69, December 1977.

49. S.G. Chamberlain, B.Y. Woo, D.B. Scott, “Modeling of Electrical Charge Injection into Charge-Coupled Devices,” *Physica Status Solidi* (a), Vol. 34, pp. 263-275, 1976.

50. S.G. Chamberlain, B.Y. Woo, “Transient Analysis of Electrical Charge Injection into Charge-Coupled Devices,” *International Journal of Electronics*, Vol. 40, pp. 569-586, 1976.

51. C.H. Chan, S.G. Chamberlain, “Numerical Methods for Charge Transfer Analysis of Charge-Coupled Devices,” *Solid-State Electronics*, Vol. 17, pp. 491-499, 1974.

52. R.C. Varshney, D.J. Roulston, S.G. Chamberlain, “Some Properties Concerning the a.c. Impedence of p-i-n and p-n-n+ Diodes,” *Solid-State Electronics*, Vol. 17, pp. 699-706, 1974.

53. C.H. Chan, S.G. Chamberlain, “A CCD Serial to Parallel Shift Register,” *IEEE Journal of Solid-State Circuits*, Vol. SC-8, pp. 388-391, October 1973.

54. R.W. Brown, S.G. Chamberlain, “Quantum Efficiency of a Silicon Gate Charge Coupled Imaging Array,” *Physica Status Solidi*, Vol. 20, pp. 657-685, December 1973.

55. S.G. Chamberlain, M.A. Copeland, A.A. Ibrahim, “Some General Experimental Studies on Charge Coupled Device Circuits,” *International Journal of Electronics*, Vol. 35, pp. 833-846, 1973.

56. R.C. Varshney, D.J. Roulston, S.G. Chamberlain, “Determination of neutral region carrier concentrations in p-n junctions using Quasi-Fermi levels,” *International Journal of Electronics*, Vol. 3, pp. 15-23, July 1973.

57. J.C. Tandon, D.J. Roulston, S.G. Chamberlain, “Reverse-bias characteristics of a P+-N-N+ Photodiode,” *Solid State Electronics*, Vol. 15, pp. 669-685, 1972.

58. D.J. Roulston, S.G. Chamberlain, J. Seghal, “Simplified Computer-Aided Analysis of Double-Diffused Transistors Including Two-Dimensional High Level Effects,” *IEEE Transactions on Electron Devices*, Vol. ED-19, No. 6, pp. 809-820, 1972.

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C. LIST OF SHORT PAPERS PUBLISHED IN REFEREED JOURNALS

1. C.N. Anagnostopoulos, T. Foxall, S.G. Chamberlain, “Introduction to the Special Issue on Technologies for Custom I.Cs (Invited),” *IEEE Journal of Solid-State Circuits*, Vol. SC-21, pp. 423-426, 1986.

2. C.N. Anagnostopoulos, S.G. Chamberlain, “Introduction to the Special Issue on Technologies for Custom I.Cs (Invited),” *IEEE Journal of Solid-State Circuits*, Vol. CS-20, pp. 467-468, 1985.

3. C.N. Anagnostopoulos, S.G. Chamberlain, “Introduction to the Special Issue on Technologies for Custom I.Cs (Invited),” *IEEE Transactions on Electron Devices*, Vol. ED-31, pp. 137-138, 1984.

4. G.S. Schlig, S.G. Chamberlain, “Output Structure for buried-channel CCD,” *IEEE Transactions on Electron Devices*, Vol. ED-31, pp. 1907-1908, December 1984.

5. N.D. Arora, D.J. Roulston, S.G. Chamberlain, “Distribution profile of diffused layer in silicon,” *Solid-State Electronics*, Vol. 25, pp. 965-967, 1982.

6. R. Kumar, D.J. Roulston, S.G. Chamberlain, “Accurate Two-Dimensional Simulation of Double-Beveled p-n Junctions,” *Solid-State Electronics*, Vol. 24, pp. 377-379, 1981.

7. N.D. Arora, S.G. Chamberlain, D.J. Roulston, “Diffusion Length Determination in p-n Junction Diodes and Solar Cells,” *Journal of Applied Physics Letters*, Vol. 37, No. 3, pp. 325-326, August 1980.

8. N.H. El-Diway, D.J. Roulston, S.G. Chamberlain, “Piecewise Linear CAD Model for Avalanche Photodetectors,” *IEEE Proceedings*, Vol. 67, No. 8, pp. 1163-1165, August 1979.

9. S.G. Chamberlain, D.J. Roulston, S.P. Desai, “Optical Silicon Lifetime Measurements in Heavily Doped Diffused Regions,” *Electronics Letters*, Vol. 13, No. 18, pp. 544-545, September 1977.

10. D.B. Scott, S.G. Chamberlain, “A Model for Charge Transport in Surface Channel Devices,” *IEEE Journal of Solid-State Circuits*, Vol. SC-11, pp. 422-424, 1976.

11. C.H. Chan, S.G. Chamberlain, “A CCD serial to parallel shift register,” *IEEE Journal of Solid-State Circuits*, Vol. SC-8, pp. 388-391, October 1973.

12. S.G. Chamberlain, V.J. Aggarwal, “Photosensitivity and Characterization of a Solid State Integrating Photodetector,” *IEEE Journal of Solid State Circuits*, Vol. SC-7, No. 2, pp. 202-204, 1972.

13. D.J. Roulston, S.G. Chamberlain, “Variation of Transistor Base Resistance and Current Gain,” *Electronics Letters*, Vol. 7, pp. 438-440, 1971.

14. S.G. Chamberlain, “Some New Properties of the Forward Biased Emitter-Base Junction of Gigahertz Silicon Transistors,” *Electronics Letters*, Vol. 6, pp. 843-845, 1970.

15. S.G. Chamberlain, G.A. Kerkut, “Voltage Clamp Studies on Helix Aspersa Neurones,” *Nature London*, Vol. 216, pp. 89, 1967.

16. S.G. Chamberlain, G.A. Kerkut, B.H. Venning, “Negative Capacitance Solid-State Microelectronic Input Circuit for use in Neurophysiology,” *Life Science*, Vol. 5, pp 743-745, 1966.

D. PARTIAL LIST OF PAPERS IN REFEREED CONFERENCE PROCEEDINGS

1. W.D. Washkurak, S.G. Chamberlain, “A floating fate dynamic range photodetector,” *IEEE Charge-Coupled Devices International Workshop*, Waterloo, Ontario, Proceedings, pp. 91-102, June 1993.

2. W.D. Washkurak, S.G. Chamberlain, “A one dimensional buried channel simulator,” *IEEE Charge-Coupled Devices International Workshop*, Waterloo, Ontario, Proceedings, pp. 120-132, June 1993.

3. S.G. Chamberlain, S.J. Strunk, S.R. Kamasz, F. Ma, W.D. Washkurak, P.T. Jenkins, M. Farrier, “25 Million Pixel CCD Image Sensor*,” International Society for Optical Engineering*, SPIE, January 31, February 4, 1993, San Jose, CA.

4. W.D. Washkurak, S.J. Strunk, S.G. Chamberlain, J.W. Roberts, “A Two Poly Lateral Antiblooming Area Array Image Sensor*,” International Society for Optical Engineering*, SPIE, January 31-February 4, 1993, San Jose, CA.

5. S.R. Kamasz, W.D. Washkurak, G.P. Weale, C.R. Smith, S.G. Chamberlain, “Design and Electro-Optical Characterization of the DALSA 1024 x 1024 CCD Imager,” *International Society for Optical Engineering*, SPIE, January 31-February 4, 1993, San Jose, CA.

6. W.D. Washkurak, S.G. Chamberlain, “A Large Pitch 128 x 256 Pixel Area Array Imager Sensor with 64 Outputs,” *International Society for Optical Engineering*, SPIE, January 31-February 4, 1993, San Jose, CA.

7. J.W. Roberts, S.D. Rose, G. Jullien, L. Nichols, P.T. Jenkins, S.G. Chamberlain, G. Maroscher, R. Mantha, D.J. Litwiller, “A PC-based Real Time Defect Imaging System for High Speed WCB Inspection,” *International Society for Optical Engineering*, SPIE, January 31-February 4, 1993, San Jose, CA.

8. S.G. Chamberlain, B.C. Doody, “CCD Image Sensor Technology,” *Canadian Conference on Electrical and Computer Engineering, Proceedings*, Toronto, ON, pp. 1-6, September 13-16, 1992.

9. D.A.B. Dobson, S.G. Chamberlain, “Transient Analysis of Signal Transfer in Long Diffused regions of Spectroscopic Image Sensors*,” Sixth Canadian Semiconductor Technology Conference*, Ottawa, ON, August 11-13, 1992.

10. P.T. Jenkins, S.G. Chamberlain, “Ultra High Speed CCD Image Sensor Technology for Image Capture,” *ISAIT International Conference on Advanced Image Technology, Proceedings – ITEC’92*, Sapporo, Japan, pp. 543-547, July 27-31, 1992.

11. S.J. Strunk, W.D. Washkurak, S.G. Chamberlain, J.R.F. McMacken and S.R. Kamasz, “Development of a multi-output 2048 x 2048 pixel CCD imager for aerial reconnaissance,” *Soc. Phot. Optical-Instrumentation Eng. Conference on Airborne Reconnaissance, Proceedings*, Vol. 1763, pp. 1-12, San Diego, CA, July 21-22, 1992.

12. W.D. Washkurak, S.J. Strunk, S.G. Chamberlain, “A Small Format 256 x 256 Full Frame Area Array Image Sensor with on-chip clocking and bias condition,” *Soc. Phot. Optical-Instrumentation Eng. Solid-State imaging, Proceedings*, San Jose, CA, pp. 1-12, February 12-14, 1992.

13. W..D. Washkurak, S.J. Strunk, S.G. Chamberlain, J.R.F. McMacken, “Surface Channel Clock Antiblooming operation with area array CCD image sensors,” *Soc. Phot. Optical-Instrumentation Eng. Solid-State imaging, Proceedings*, San Jose, CA, pp. 1-16, February 12-14, 1992.

14. S.G. Chamberlain, “CCD Time-Delay-and-Integration Imagers (Invited),” *Symposium on Advanced Image-Acquisition 1991, Proceedings*, Tokyo, Japan, pp. 1-16, November 12-14, 1991.

15. S.G. Chamberlain, J.R.F. McMacken, “Semiconductor Device Simulation for CCDs using the Drift-Diffusion and Hydrodynamic Formulation,” *IEEE Charge-Coupled Devices Workshop, Proceedings*, University of Waterloo, Waterloo, ON, pp. 1-42, June 7-9, 1991.

16. S.G. Chamberlain, J.R.F. McMacken, J.W. Roberts, “An Impact Ionization Model for Two-Carrier Energy-Momentum Simulator,” *4th International Conference on Simulation of Semiconductor Devices and Processes, Proceedings*, Zurich, pp. 1-12, September 1991.

17. J.W. Roberts, S.G. Chamberlain, J.R.F. McMacken, “Energy-Momentum Transport Simulator Adapted to CHORD,” *Proceedings of the Canadian Technology Conference*, pp. 1-2, Ottawa, ON, August 1990.

18. S.J. Hood, S.G. Chamberlain, “Colour Filter Arrays for Silicon Solid-State Image Array Sensors,” *Proceedings of the Canadian Technology Conference*, pp. 1-2, Ottawa, ON, August 1990.

19. S.G. Chamberlain, W.D. Washkurak, “High-Speed, Low Noise, Fine Resolution TDI CCD Imagers,” *Proceedings, Charge-Coupled Devices and Solid-State Sensors*, Vol. 1242, pp. 252-262, February 12-14, 1990.

20. S.G. Chamberlain, “Advanced CCD Image Sensor Technology Made in Canada,” *Proceedings of the Canadian Conference on Electrical and Computer Engineering*, pp. 1-2, September 4-6, 1990.

21. J.W. Roberts, S.G. Chamberlain, “Energy-Momentum Transport Computer Simulator for VLSI Device Structures,” *Proceedings of the 1990 IEEE VLSI Process/Device Modelling Workshop*, pp. 106-107, Kawasaki, Japan, August 21-22, 1990.

22. S.G. Chamberlain, W.D. Washkurak, “High Speed low noise fine resolution Time-delay-and-Integration CCD Imagers (Invited),” *Soc. Phot. Optical-Instrumentation Eng. Conference Proceedings, Charge-Coupled Devices and Solid-State Optical Sensors*, Vol. 1242, pp. 252-262, February 12-14, 1990.

23. W.D. Washkurak, S.G. Chamberlain, P.T. Jenkins, “A Time delay and Integration CCD Image Sensor for High Speed and Low light Level Scanning Applications,” *Electronic Imaging 89*, Pasadena, CA, pp. 562-566, April 10-13, 1989.

24. S.G. Chamberlain, W.D. Washkurak, “Wide Dynamic range CCD area image sensor,” *Soc. Phot. Optical-Instrumentation Eng., Optical and Opto-electronic Applied Science and Engineering*, Vol. 1168-37, San Diego, CA, pp. 1-5, August 6-11, 1989.

25. S.G. Chamberlain, B.C. Doody, W.D. Washkurak, “CCD Time Delay and Integration Imager,” *Electronic Imaging*, Vol. 2, Boston, October 2-5, 1989.

26. S.G. Chamberlain, “High Speed Image Sensors for Robots and Computer Vision (Invited),” *Soc. Phot. Optical-Instrumentation Eng. Symposium, Image Sensing for Machine Vision*, Vol. 1194, Philadelphia, November 8-10, 1989.

27. W.D. Washkurak, S.G. Chamberlain, N.D. Prince, “High Speed wide dynamic range linear CCD detector for acousto-Optic applications,” *Soc. Phot. Optical-Instrumentation Eng. Symposium on Advances in Optical Information Processing*, Orlando, FL, pp. 1-9, April 4-8, 1988.

28. R. Inkol, W.D. Washkurak, S.G. Chamberlain, “Tapped high speed image sensor,” *4th Canadian Semiconductor Technology*, Ottawa, August 9-11, 1988.

29. W.D. Washkurak, B.C. Doody, S.G. Chamberlain, “A wide dynamic range tapped linear array image sensor,” *Soc. Phot. Optical-Instrumentation Eng. Conference Proceedings*, Vol. 972, pp. 33-38, 1988.

30. L.R. Hudson, C.R. Chung, S.G. Chamberlain, W.D. Washkurak, “High-Speed High-Dynamic Range Linear Array,” *Soc. Phot. Optical-Instrumentation Eng. Conference Proceedings*, Vol. 972, pp. 33-38, 1988.

31. S.G. Chamberlain, B.C. Doody, W.D. Washkurak, “A high photosensitivity wide dynamic range linear image sensor array,” *Electronic Imaging*, Anaheim, CA, pp. 170-175, March 28-31, 1988.

32. S.G. Chamberlain, W.D. Washkurak, B.C. Doody, “CCD Image sensors for high speed inspection systems,” *Soc. Phot. Optical-Instrumentation Eng. Advances in Intelligent Robotic Systems, Conference Proceedings*, Cambridge, MASS, pp. 1-10, November 1-6, 1987.

33. B.C. Doody, S.G. Chamberlain, W.D. Washkurak, “A high photosensitivity wide dynamic range silicon linear image sensor array,” *Proceedings of Electronic Imaging 87*, Boston, MASS, pp. 1-5, November 3-5, 1987.

34. S.G. Chamberlain, S. Ramanan, “VTMOS, A two-dimensional program for the threshold voltage and subthreshold current of VLSI MOSFET devices,” *Proceedings IEEE Custom Integrated Circuits Conference*, Rochester, NY, pp. 212-215, May 12-14, 1986.

35. S.G. Chamberlain, Y.L. Yao, D. Higa, “A charge coupled device model for computer simulations,” *Proceedings IEEE International Symposium on Circuits and Systems*, San Jose, CA, pp. 165-169, May 5-7, 1986.

36. B.C. Doody, S.G. Chamberlain, “A Novel silicon photodetector with wide dynamic range operation in practical sensor arrays,” *Proceedings of the SPSE International Conference on Electronic Imaging*, Washington, D.C., pp. 107, October 14-17, 1986.

37. S.G. Chamberlain, J.H. Broughton, “Technology Progress and Trends in Solid-State Image Sensors (Invited),” *Proc. IEEE Custom Integrated Circuits Conference*, Portland, OR, pp. 112-118, May 1985.

38. S. Ramanan, S.G. Chamberlain, “Drain Induced barrier Lowering Limitations in VLSI MOSFET Devices,” *Proceedings of the 6th Biennial Microelectronics Symposium*, Auburn, AB, pp. 138-143, 1985.

39. S.G. Chamberlain, J.P.Y. Lee, “Silicon Imaging arrays with new photoelectronics, wide dynamic range and free from blooming,” *Proc. IEEE Custom I.C. Conference*, Rochester, NY pp. 81-85, 1984.

40. S.G. Chamberlain, J.P.Y Lee, “A Novel Wide Dynamic range Photodetector and linear Imaging Array,” *Proc. IEEE Custom I.C. Conference*, Rochester, NY, pp. 441-445, 1983.

41. S.G. Chamberlain, “Two and Three dimensional simulation for VLSI MOSFETs (Invited),” *Proc. IEEE International Symposium on VLSI Tech*nology, Taipei, R.O.C., pp. 94-98, 1983.

42. S.G. Chamberlain, A. Husain, “The need for 3D Simulation for VLSI MOSFETs, CCD Imagers and CCD SPS Memories*,” Proceedings IEEE Custom Integrated Circuits Conference*, Rochester, NY, pp. 191-195, 1982.

E. PARTIAL LIST OF SEMINARS GIVEN BY INVITATION AND GUEST SPEAKER TALKS

1. Savvas Chamberlain, Guest Speaker **“The Evolution of CCD and CMOS Sensor and Camera Technologies for Industrial Applications”** Parameter Jubilee, Stockholm, Sweden, September 19, 2007.

2. Savvas Chamberlain, Guest Speaker **"The Evolution of CCD and CMOS Sensor and Camera Technologies for Industrial Applications"** China Vision Trade Show, Beijing, PRC, June 11, 2006.

3. Savvas Chamberlain, Guest Speaker, "**A Brief History of the Evolution of DALSA Corporation**" Auburn University, Auburn, AL, February 21, 2006.

4. Savvas Chamberlain, Guest Speaker **"DALSA Corporation: Using Technology as a Competitive Resource in a Changing Global Economy"** Klein Symposium, Penn State University, State College, PA, October 14, 2005.

5. Savvas Chamberlain, Guest Speaker "**Technology Transfer from Research to Industry**" University of Waterloo, Center Business Engineering Technology, Waterloo, ON, March 3, 2005.

6. Savvas Chamberlain, Guest Speaker "**The contribution of DALSA Corporation to the evolution of digital imaging**" Automated Imaging Association, Annual General Meeting, Orlando, FL, February 5, 2004.

7. S.G. Chamberlain, "Advances in CCD Image Sensor Technology," Invited, *Canadian Association of Physicists, Burnaby, British Columbia*, June, 1993.

8. S.G. Chamberlain, "Simulations on small geometry Semiconductor devices, including energy-momentum formulation," Invited, *Hitachi Research Laboratory, Kokubunji, Tokyo, Japan*, November 15, 1991.

9. S.G. Chamberlain, "Wide dynamic range CCD image sensors," *JET Propulsion Laboratory, CalTech, Pasadena*, CA, October 1988.

10. S.G. Chamberlain, "CCDs for High Speed Signal Processing," *MIT-Lincoln Labs, Lexington, MASS*, October 1988.

F. SUPERVISION OF GRADUATE STUDENTS

Ph.D students supervised and graduated

1. P. Gudem, PhD, Graduated 1996, 2. S. GadelRab, PhD, Graduated 1996,
3. A.. Miri, PhD, Graduated 1996, 4. W. Washkurak, PhD, Graduated 1994,
5. C. Smith, PhD, Graduated 1992, 6. J. Roberts, PhD, Graduated 1991,
7. P.Layman, PhD, Graduated 1990, 8. J. McMacken, PhD, Graduated 1990,
9. M. van der Tol, PhD, Graduated 1990, 10.A. Husain, PhD, Graduated 1982,
11. M. El-Diwany, PhD, Graduated 1981, 12. D.B. Scott, PhD, Graduated 1979,
13. H.A. Zohdy, PhD, (co-supervisor, L.A.K. Watt), Graduated 1977,
14. C.H. Chan, PhD, Graduated 1976, 15. R.C.Kumar,PhD,(co-supervisor, D.J. Roulston).
J. Tandon, PhD, (co-supervisor, D.J. Roulston).

MASc students supervised and graduated (By Thesis)

1. R.B. Coenen, MASc, Graduated Spring 1994, 2. C.D. McGuire, MASc, Graduated Spring 1994. 3. N. Hasani, MASc, Graduated Spring 1994, 4. S.M. GadelRab, MASc, Graduated Spring 1993, 5. D.A.B. Dobson, MASc, Graduated Spring 1992, 6. S. Agwani, MASc, Graduated Fall 1991, 7. P. Goulet, MASc, Graduated Spring 1990, 8. S. Hood, MASc, Graduated 1988, 9. C. Smith, MASc, Graduated 1986, 10. P.A. Layman, MASc,

11. W. Washkurak, MASc, Graduated 1985, 12. D.B. Scott, MASc, Graduated 1985,
13. P. Tsui, MASc, Graduated 1984, 14. S. Dondale, MASc, Graduated 1980,
15. R. Inkol, MASc, Graduated 1978, 16. P. Desai, MASc, Graduated 1977,
17. D. Harper, MASc, Graduated 1976, 18. E.A. Hall, MASc, Graduated 1976,
19. F. Gordeau, MASc. 20. H.A. Zohdy, MASc. 21. V.J. Aggarwal, MASc.
22. R.W. Brown, MASc. 23. P.S. Leung, MASc. 24. D.R. Wilson, MASc.
25. R. Chow, MASc. 26. L. Greggain, MASc. 27. L. McKinly, MASc.
28. M. Kulas, 1995 (co-supervisor, A. Nathan), MASc.
29. I. Lian, 1995 (co-supervisor, R.I. Hornsey

G. MEMBERSHIP ON PROFESSIONAL COMMITTEES AND JOURNAL EDITORIAL BOARDS

1. Member of the Canadian Academies Panel on Business Innovation 2008.

2. NCR Microelectronics Fellowship to carry out research at the University of Waterloo, January 1991- December 1994.

3. Member of the organizing committee of the IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Bruges, Belgium, 1995-1997.

4. Chairman and organizer of the International IEEE CCD Workshop held at the University of Waterloo, June 1991.

1. Member of the selection and site visit committee of strategic grants, 1988.

2. Member of an NSERC committee for NSERC-BNR chairs(2), 1988-1992.

3. Member of the Area Microelectronics committee of the Information Technology Research Centre(Ontario Centre of Excellence), 1987 – 1992.

4. Member of the committee of Microelectronics and Principal Investigator, Federal Center of Excellence, MICRONET, 1988-1992.

5. Associate Editor of the *IEEE Journal of Solid-State Circuits*, 1984-1988.

6. General Chairman of the IEEE CICC International Conference, 1986-1987.
Chairman of the NSERC Operating Grant Selection Committee, Electrical Engineering 1988-1989.

7. Vice Chairman of the NSERC Operating Grant Selection Committee, Electrical Engineering, 1987-1988.

8. Member of the NSERC Operating Grant Selection Committee, Electrical Engineering, 1986-1987

9. Member of the OGS Scholarship Committee, 1982-1983.

10. Guest Editor of the *IEEE Transactions on Electron Devices*, 1978, 1984.

11. Member of the Editorial Board of *Electronic Imaging*, 1982-1984.

12. Chairman of the IEEE CICC International Conference, 1984-1985.

13. Technical Program Chairman for the IEEE CICC International Conference, 1982-1983.

14. Member of the organization committee of the IEEE CICC International Conference, 1979-1987.

END